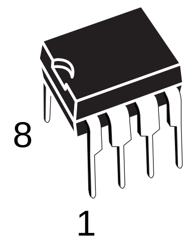
M95040
M95020, M95010

4Kbit, 2Kbit and 1Kbit Serial SPI Bus EEPROM With High Speed Clock

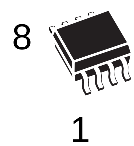
FEATURES SUMMARY

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage:
  - 4.5V to 5.5V for M950x0
  - 2.5V to 5.5V for M950x0-W
  - 1.8V to 3.6V for M950x0-S
- 5 MHz Clock Rate (maximum)
- Status Register
- BYTE and PAGE WRITE (up to 16 Bytes)
- Self-Timed Programming Cycle
- Adjustable Size Read-Only EEPROM Area
- Enhanced ESD Protection
- More than 1,000,000 Erase/Write Cycles
- More than 40 Year Data Retention

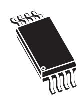
Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width

SUMMARY DESCRIPTION

The M95040 is a 4 Kbit (512 x 8) electrically erasable programmable memory (EEPROM), accessed by a high speed SPI-compatible bus. The other members of the family (M95020, M95010) are identical, though proportionally smaller (2 and 1 Kbit, respectively).

Each device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in Table 1 and Figure 2.

The device is selected when Chip Select ($\overline{\text{S}}$) is taken Low. Communications with the device can be interrupted using Hold ($\overline{\text{HOLD}}$). WRITE instructions are disabled by Write Protect ($\overline{\text{W}}$).

Figure 2. Logic Diagram

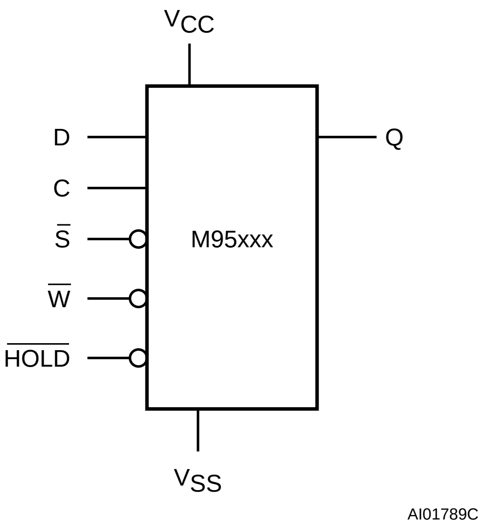
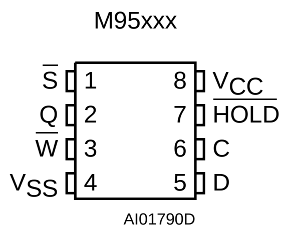


Figure 3. DIP, SO and TSSOP Connections



Note: 1. See page 28 (onwards) for package dimensions, and how to identify pin-1.

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{\text{S}}$	Chip Select
$\overline{\text{W}}$	Write Protect
$\overline{\text{HOLD}}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

SIGNAL DESCRIPTION

V_{CC} must be held within the specified range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held High or Low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in Tables 12 to 16). These signals are described next.

Serial Data Output (Q)

This output signal is used to transfer data serially out of the device. Data bytes are shifted out on the falling edge of the Serial Clock (C).

Serial Data Input (D)

This input signal is used to transfer data serially into the device. Instructions, addresses, and input data bytes are shifted in on the rising edge of the Serial Clock (C).

Serial Clock (C)

This input signal provides the timing for the serial interface.

Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected, and the Serial Data Output (Q) is high impedance.

Hold ($\overline{HOLD}$)

This input signal is used to pause temporarily any serial communications with the device, without losing bits that have already been passed on the serial bus.

Write Protect ($\overline{W}$)

This input signal is used to control whether the memory is write protected. When $\overline{W}$ is held Low, writes to the memory are disabled, but other operations remain enabled. No action on this signal, or on the Write Enable Latch (WEL) bit, can interrupt a Write cycle that has already started.

CONNECTING TO THE SPI BUS

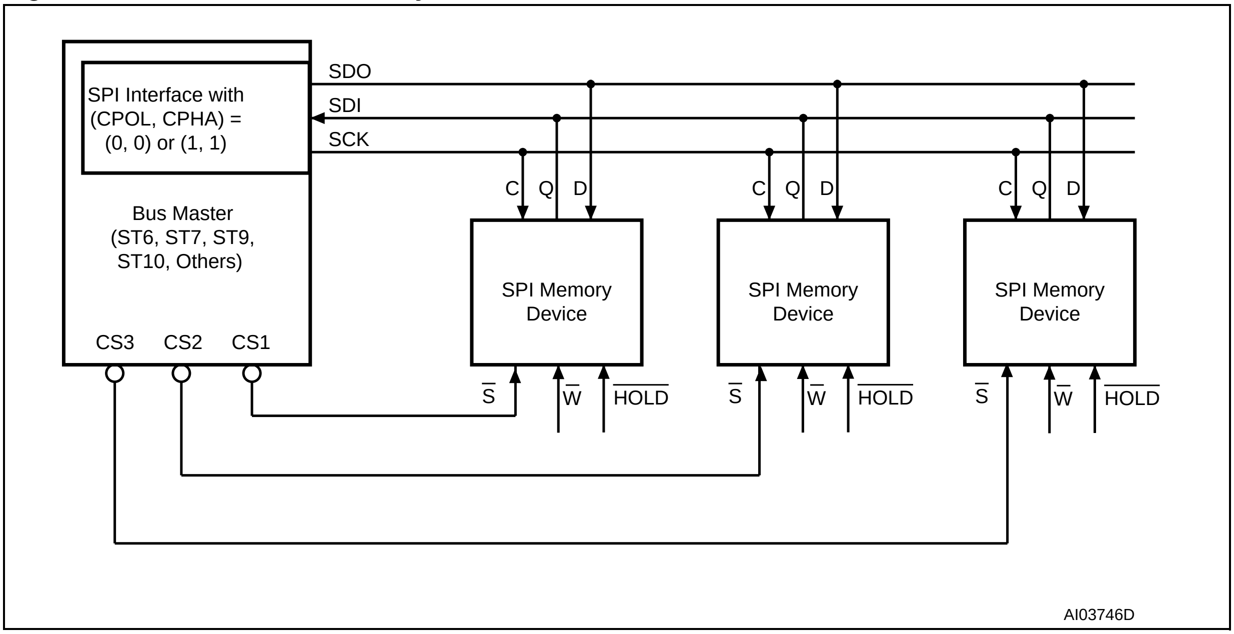
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes Low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 4 shows three devices, connected to an MCU, on a SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, all the others being high impedance.

Figure 4. Bus Master and Memory Devices on the SPI Bus



Note: 1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

– CPOL=0, CPHA=0

– CPOL=1, CPHA=1

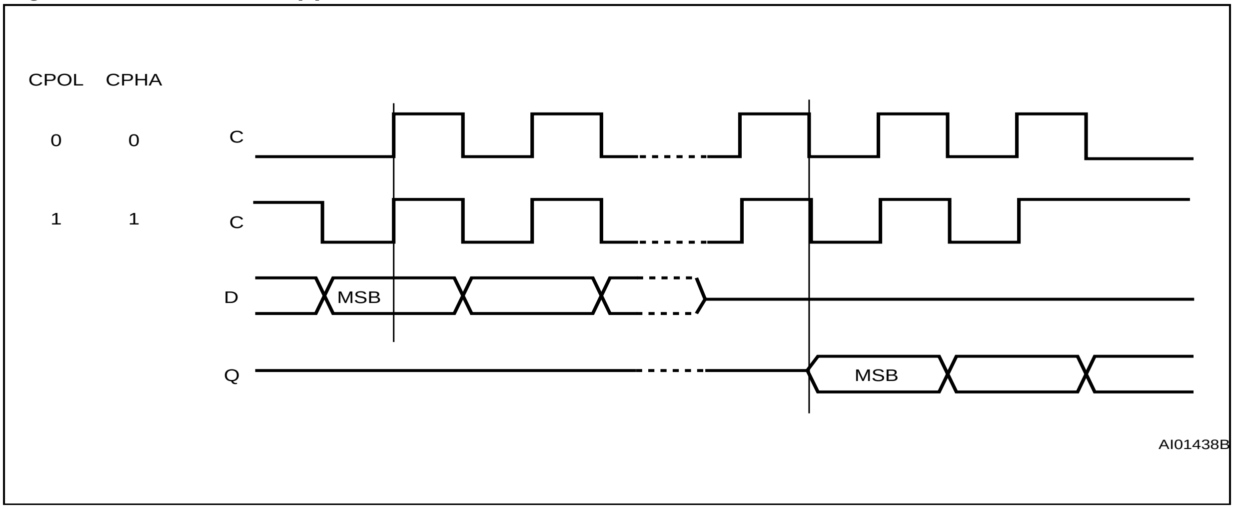
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 5, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

– C remains at 0 for (CPOL=0, CPHA=0)

– C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. SPI Modes Supported



OPERATING FEATURES

Power-up

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}.

During this time, the Chip Select ($\overline{S}$) must be allowed to follow the V_{CC} voltage. It must not be allowed to float, but should be connected to V_{CC} via a suitable pull-up resistor.

As a built in safety feature, Chip Select ($\overline{S}$) is edge sensitive as well as level sensitive. After Power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been High, prior to going Low to start the first operation.

Power-down

At Power-down, the device must be deselected. Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}.

Active Power and Stand-by Power Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode. The device consumes I_{CC}, as specified in Tables 12 to 16.

When Chip Select ($\overline{S}$) is High, the device is disabled. If an Erase/Write cycle is not currently in progress, the device then goes in to the Stand-by Power mode, and the device consumption drops to I_{CC1}.

Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

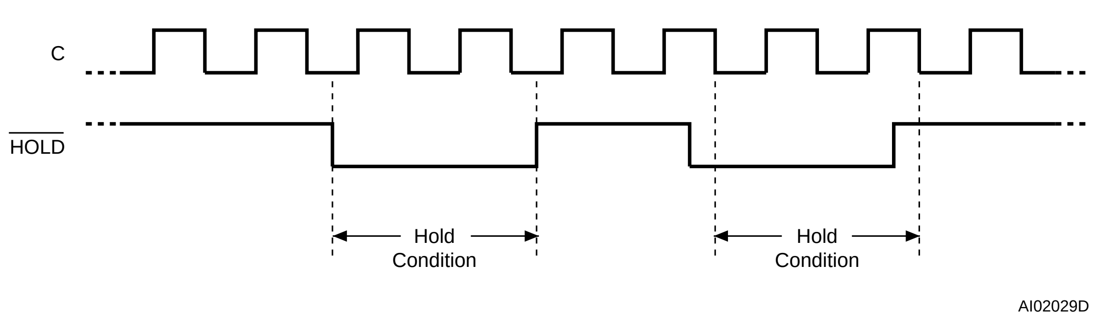
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven Low at the same time as Serial Clock (C) already being Low (as shown in Figure 6).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being Low.

Figure 6 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being Low.

Figure 6. Hold Condition Activation



Status Register

Figure 7 shows the position of the Status Register in the control logic of the device. This register contains a number of control bits and status bits, as shown in Table 2.

Bits b7, b6, b5 and b4 are always read as 1.

WIP bit. The Write In Progress bit is a volatile read-only bit that is automatically set and reset by the internal logic of the device. When set to a 1, it indicates that the memory is busy with a Write cycle.

WEL bit. The Write Enable Latch bit is a volatile read-only bit that is set and reset by specific instructions. When reset to 0, no WRITE or WRSR instructions are accepted by the device.

BP1, BP0 bits. The Block Protect bits are non-volatile read-write bits. These bits define the area of memory that is protected against the execution of Write cycles, as summarized in Table 3.

Table 2. Status Register Format

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

Block Protect Bits

Write Enable Latch Bit

Write In Progress Bit

Data Protection and Protocol Control

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

– The WEL bit is reset at power-up.
– Chip Select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile Write cycle (in the memory array or in the Status Register).
– Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
– Invalid Chip Select ($\overline{S}$) and Hold ($\overline{HOLD}$) transitions are ignored.

For any instruction to be accepted and executed, Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches the last bit of the instruction, and before the next rising edge of Serial Clock (C).

For this, “the last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except in the case of RDSR and READ instructions). Moreover, the "next rising edge of CLOCK" might (or might not) be the next bus transaction for some other device on the bus.

When a Write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction until the present cycle is complete.

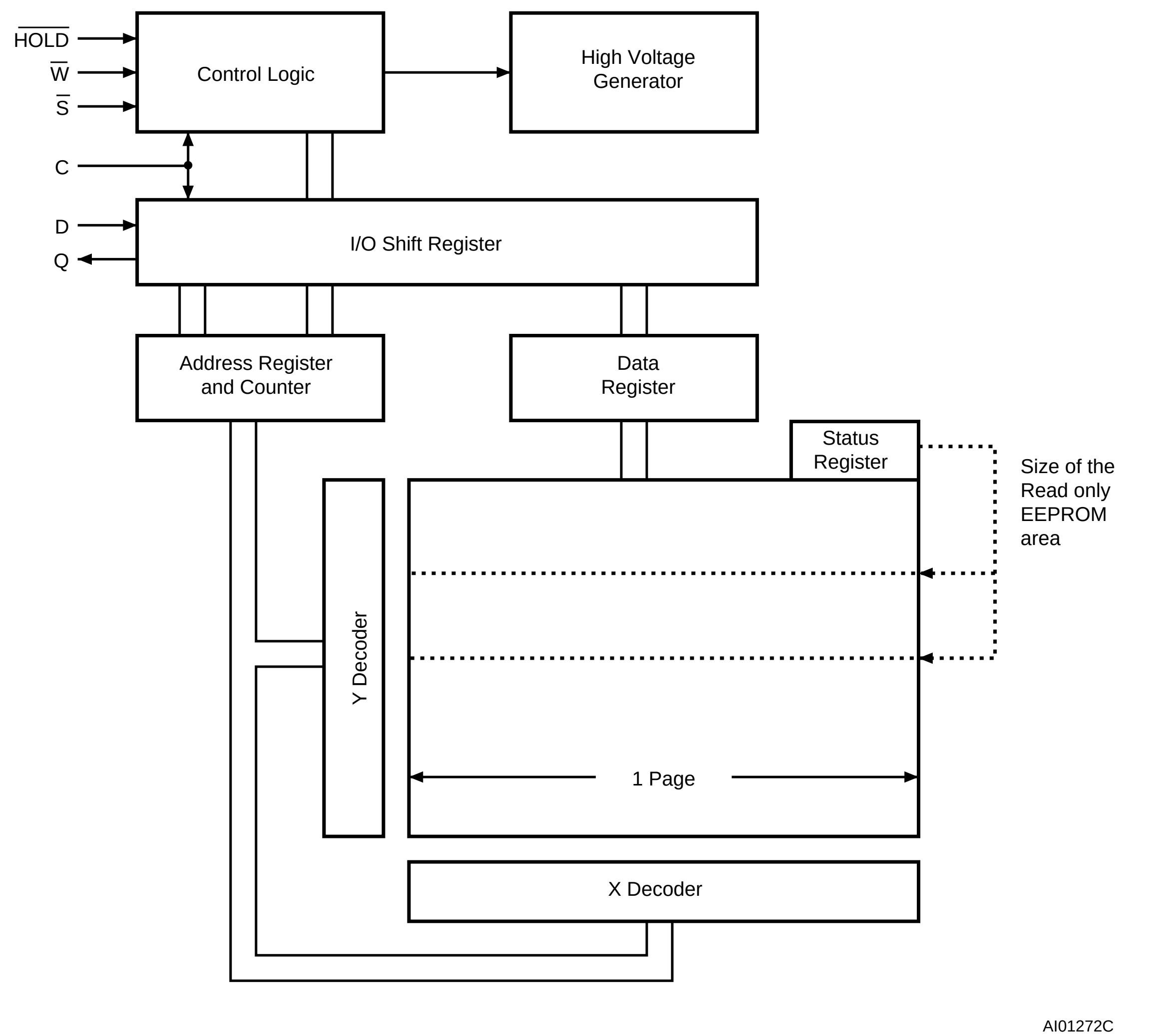
Table 3. Write-Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	060h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	040h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	000h - 7Fh

MEMORY ORGANIZATION

The memory is organized as shown in Figure 7.

Figure 7. Block Diagram



INSTRUCTIONS

Each instruction starts with a single-byte code, as summarized in Table 4.

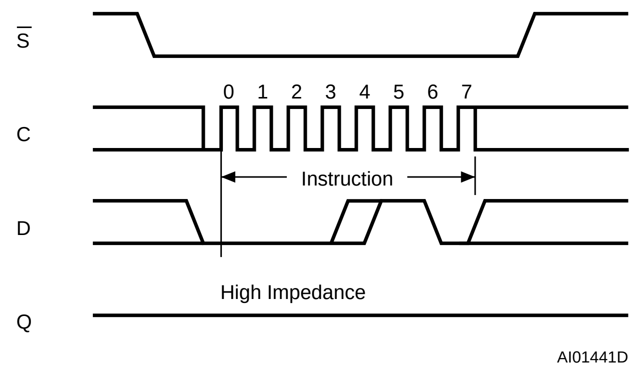
If an invalid instruction is sent (one not contained in Table 4), the device automatically deselects itself.

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 X110
WRDI	Write Disable	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read from Memory Array	0000 $A_8$011
WRITE	Write to Memory Array	0000 $A_8$010

Note: 1. A8 = 1 for the upper half of the memory array of the M95040, and 0 for the lower half, and is Don't Care for other devices.
2. X = Don't Care.

Figure 8. Write Enable (WREN) Sequence

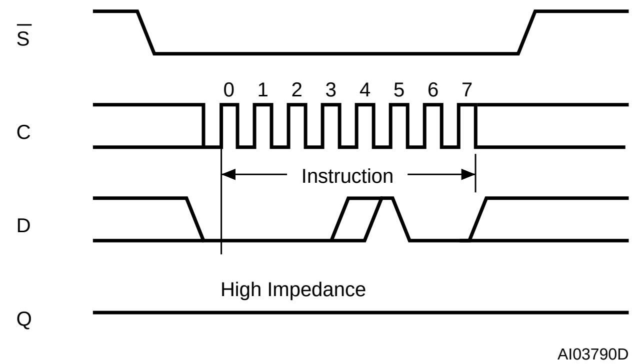


Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in Figure 8, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

Figure 9. Write Disable (WRDI) Sequence



Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

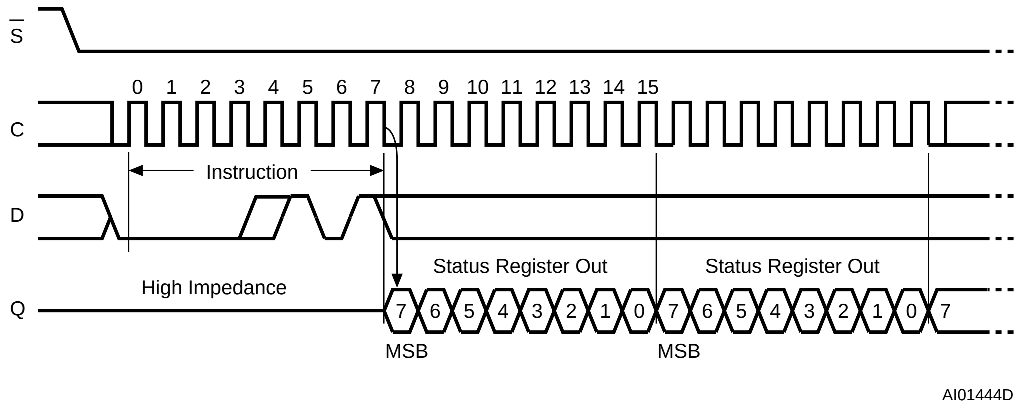
As shown in Figure 9, to send this instruction to the device, Chip Select ($\overline{S}$) is driven Low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven High.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

– Power-up
– WRDI instruction execution
– WRSR instruction completion
– WRITE instruction completion
– Write Protect ($\overline{W}$) line being held Low.

Figure 10. Read Status Register (RDSR) Sequence



Read Status Register (RDSR)

One of the major uses of this instruction is to allow the MCU to poll the state of the Write In Progress (WIP) bit. This is needed because the device will not accept further WRITE or WRSR instructions when the previous Write cycle is not yet finished.

As shown in Figure 10, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte are then shifted in, on Serial Data Input (D). The current state of the bits in the Status Register is shifted out, on Serial Data Out (Q). The Read Cycle is terminated by driving Chip Select ($\overline{S}$) High.

The Status Register may be read at any time, even during a Write cycle (whether it be to the memory area or to the Status Register). All bits of the Status Register remain valid, and can be read using the RDSR instruction. However, during the current Write cycle, the values of the non-volatile bits (BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the Write cycle. On the other hand, the two read-only bits (Write Enable Latch (WEL), Write In Progress (WIP)) are dynamically updated during the on-going Write cycle.

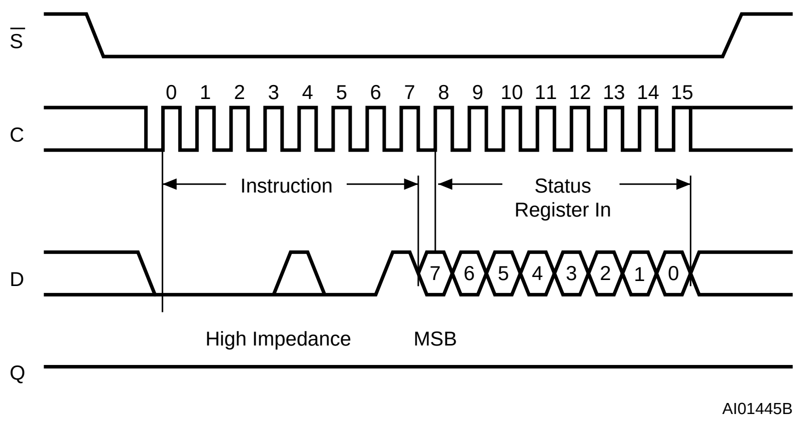
The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

BP1, BP0 bits. The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

Figure 11. Write Status Register (WRSR) Sequence



Write Status Register (WRSR)

This instruction has no effect on bits b7, b6, b5, b4, b1 and b0 of the Status Register.

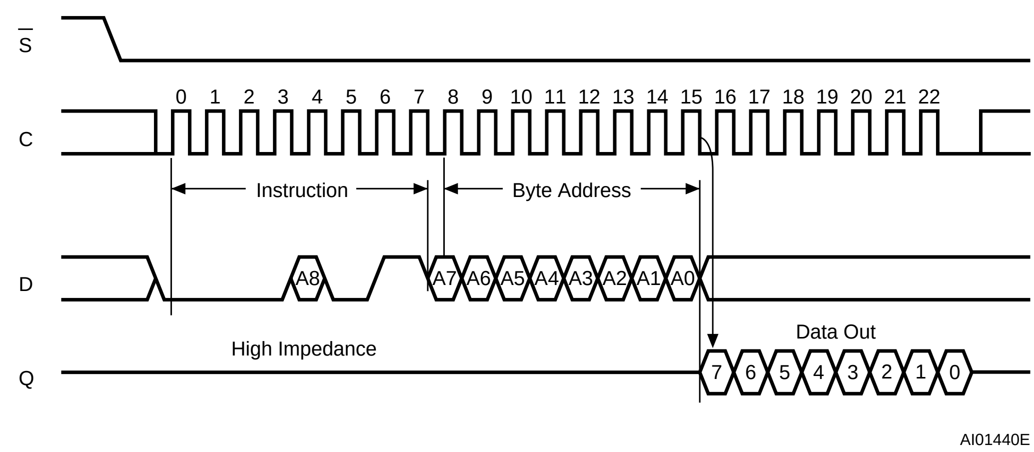
As shown in Figure 11, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and data byte are then shifted in on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) must be driven High after the rising edge of Serial Clock (C) that latches the eighth bit of the data byte, and before the the next rising edge of Serial Clock (C). If this condition is not met, the Write Status Register (WRSR) instruction is not executed. The self-timed Write Cycle starts, and continues for a period t_W (as specified in Tables 17 to 20), at the end of which the Write in Progress (WIP) bit is reset to 0.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write Cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, after the eighth bit, b0, of the data byte has been latched in
- if Write Protect ($\overline{W}$) is Low.

Figure 12. Read from Memory Array (READ) Sequence



Note: Depending on the memory size, as shown in Table 5, the most significant address bits are Don't Care.

Read from Memory Array (READ)

As shown in Figure 12, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte and address byte are then shifted in, on Serial Data Input (D). For the M95040, the most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in Table 4. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven Low, an internal bit-pointer is automatically incremented at each clock cycle, and the corresponding data bit is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) High. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

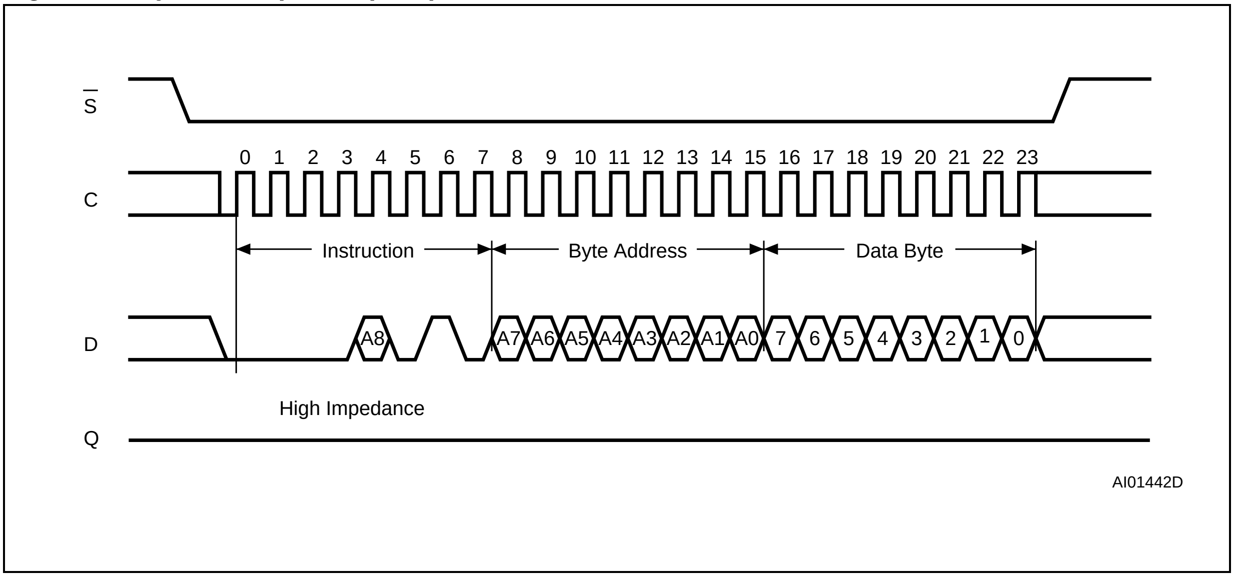
The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Table 5. Address Range Bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

Figure 13. Byte Write (WRITE) Sequence



Note: Depending on the memory size, as shown in Table 5, the most significant address bits are Don't Care.

Write to Memory Array (WRITE)

As shown in Figure 13, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven Low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) High after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus. In the case of Figure 13, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in Tables 17 to 20), at the end of which the Write in Progress (WIP) bit is reset to 0.

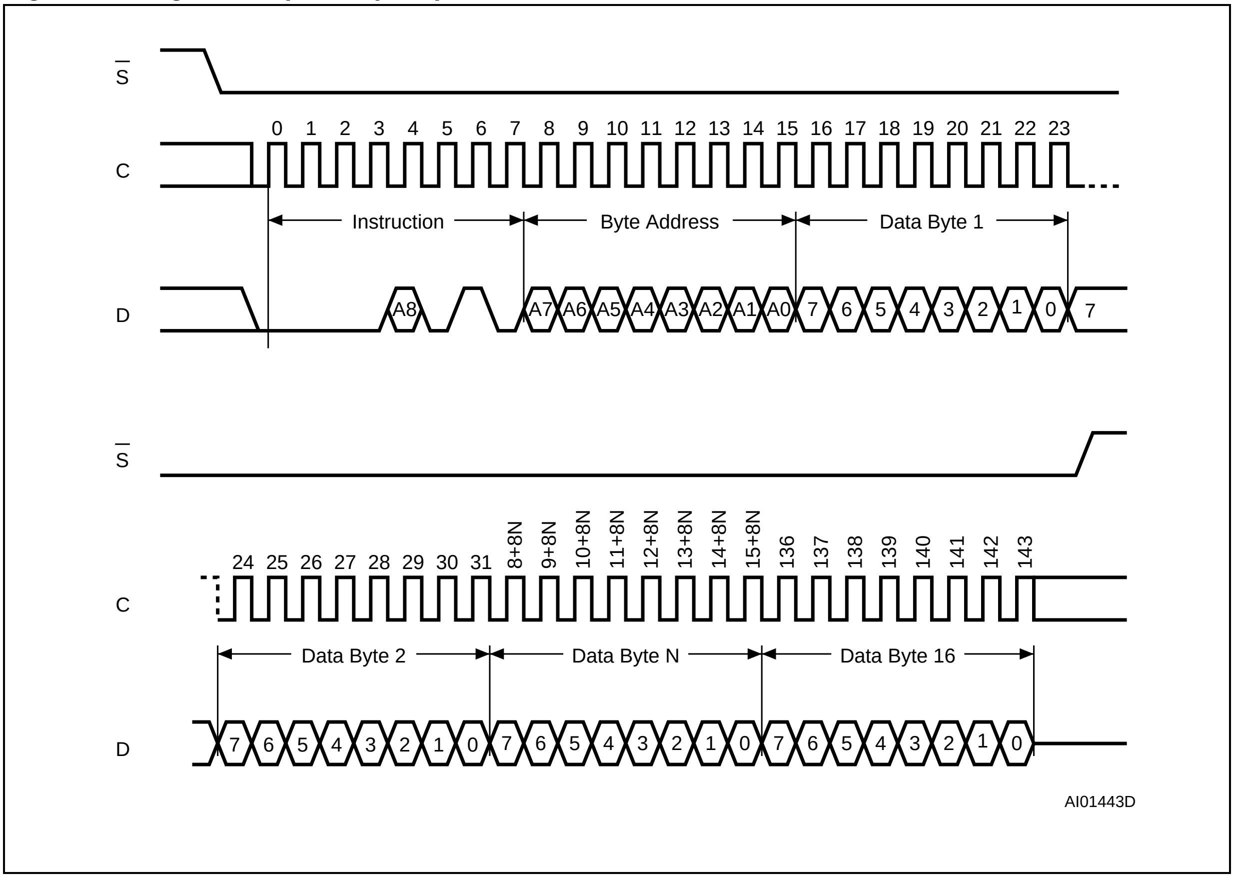
If, though, Chip Select ($\overline{S}$) continues to be driven Low, as shown in Figure 14, the next byte of input data is shifted in. In this way, all the bytes from the given address to the end of the same page can be programmed in a single instruction.

If Chip Select ($\overline{S}$) still continues to be driven Low, the next byte of input data is shifted in, and is used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

– if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
– if a Write cycle is already in progress
– if the device has not been deselected, by Chip Select ($\overline{S}$) being driven High, at a byte boundary (after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus)
– if Write Protect ($\overline{W}$) is Low or if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 14. Page Write (WRITE) Sequence



Note: Depending on the memory size, as shown in Table 5, the most significant address bits are Don't Care.

POWER-UP AND DELIVERY STATE

Power-up State

After Power-up, the device is in the following state:

– low power Stand-by mode
– deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
– not in the Hold Condition
– the Write Enable Latch (WEL) is reset to 0
– Write In Progress (WIP) is reset to 0

the BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

Initial Delivery State

The device is delivered with the memory array set at all 1s (FFh). The Block Protect (BP1 and BP0) bits are initialized to 0.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage Temperature		–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP: 10 seconds SO: 20 seconds (max) [1] TSSOP: 20 seconds (max) [1]		260 235 235	°C
V_O	Output Voltage		–0.3	V_{CC}+0.6	V
V_I	Input Voltage		–0.3	6.5	V
V_{CC}	Supply Voltage		–0.3	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		–4000	4000	V

Note: 1. IPC/JEDEC J-STD-020A
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating Conditions (M950x0)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (range 6)	–40	85	°C
	Ambient Operating Temperature (range 3)	–40	125	°C

Table 8. Operating Conditions (M950x0-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (range 6)	–40	85	°C
	Ambient Operating Temperature (range 3)	–40	125	°C

Table 9. Operating Conditions (M950x0-S)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	3.6	V
T_A	Ambient Operating Temperature	–20	85	°C

Table 10. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 15. AC Measurement I/O Waveform

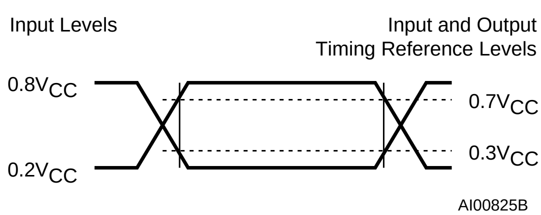


Table 11. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (D)	V_{IN} = 0V		8	pF
	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 5 MHz.

Table 12. DC Characteristics (M950x0, temperature range 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply Current (Stand-by)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}[1]	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}[1]	Output High Voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V

Note: 1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 13. DC Characteristics (M950x0, temperature range 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply Current (Stand-by)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}[1]	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}[1]	Output High Voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V

Note: 1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 14. DC Characteristics (M950x0-W, temperature range 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 2 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply Current (Stand-by)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

Table 15. DC Characteristics (M950x0-W, temperature range 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 2 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply Current (Stand-by)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		5	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

Table 16. DC Characteristics (M950x0-S)

Symbol	Parameter	Test Condition	Min.[1]	Max.[1]	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9. V_{CC} at 1 MHz, V_{CC} = 1.8 V, Q = open		2	mA
I_{CC1}	Supply Current (Stand-by)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 1.8 V		2	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

Note: 1. Preliminary data, for the 1.8V to 3.6 supply voltage range devices.

Table 17. AC Characteristics (M950x0, temperature range 6)

Test conditions specified in Table 10 and Table 7					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock Frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		ns
t_{CH} [1]	t_{CLH}	Clock High Time	90		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	90		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	60		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	60		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		100	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		50	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		50	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100	ns
t_W	t_{WC}	Write Time		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 18. AC Characteristics (M950x0, temperature range 3)

Test conditions specified in Table 10 and Table 7					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock Frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	100		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	100		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	100		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		ns
t_{CH} [1]	t_{CLH}	Clock High Time	200		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	200		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	100		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	90		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	120		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	120		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		150	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		100	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		100	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		150	ns
t_W	t_{WC}	Write Time		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 19. AC Characteristics (M950x0-W, temperature ranges 6 and 3)

Test conditions specified in Table 10 and Table 8					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		ns
t_{CH} [1]	t_{CLH}	Clock High Time	200		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	200		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	140		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	90		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	120		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	120		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		100	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		100	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250	ns
t_W	t_{WC}	Write Time		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 20. AC Characteristics (M950x0-S)

Test conditions specified in Table 10 and Table 9					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock Frequency	D.C.	1	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	400		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	300		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	400		ns
t_{CH} [1]	t_{CLH}	Clock High Time	400		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	400		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	100		ns
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	350		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	200		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	250		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	250		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		200	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		200	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		250	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		500	ns
t_W	t_{WC}	Write Time		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Figure 16. Serial Input Timing

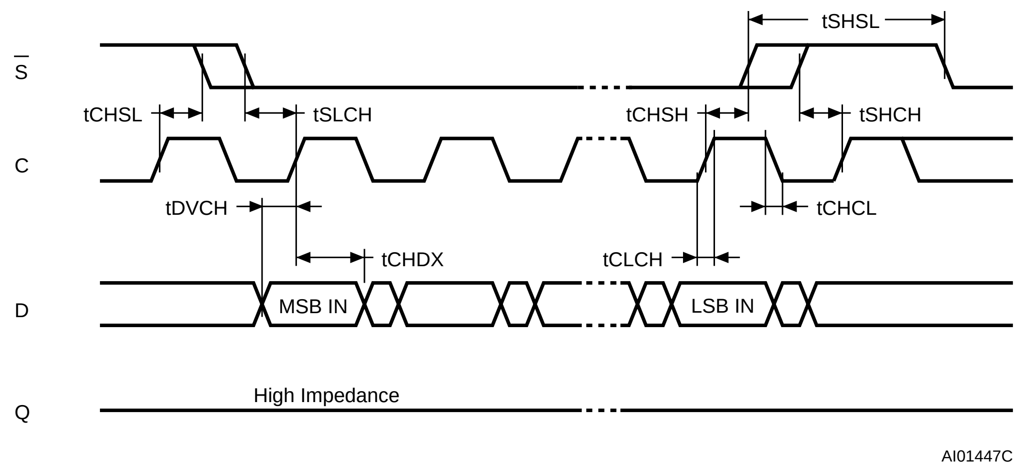


Figure 17. Hold Timing

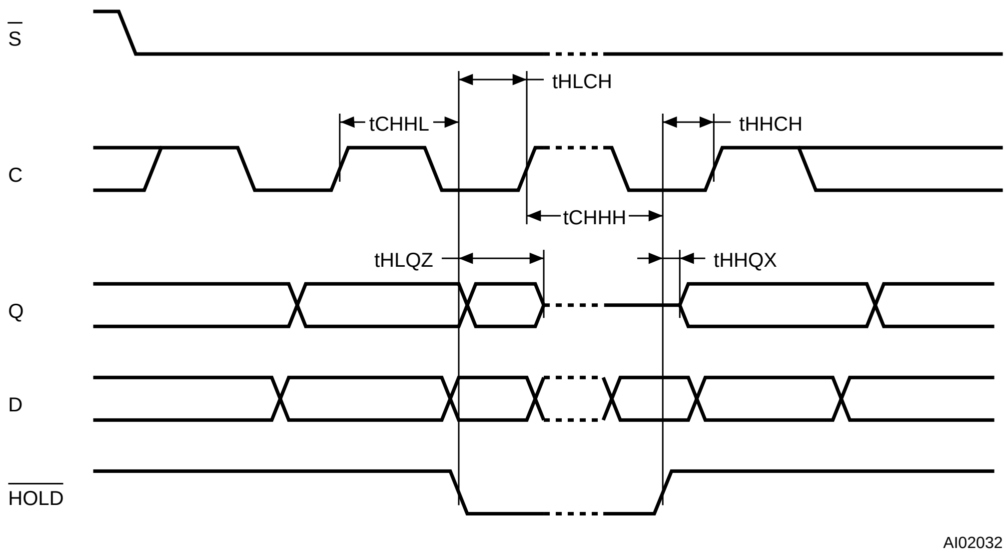
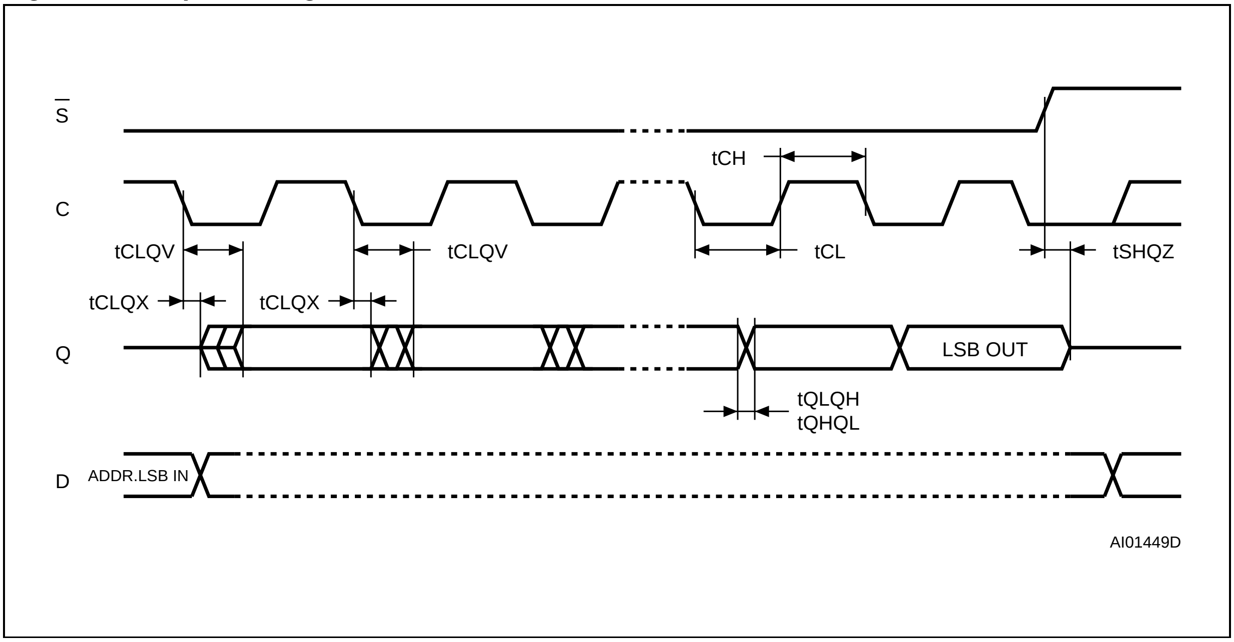
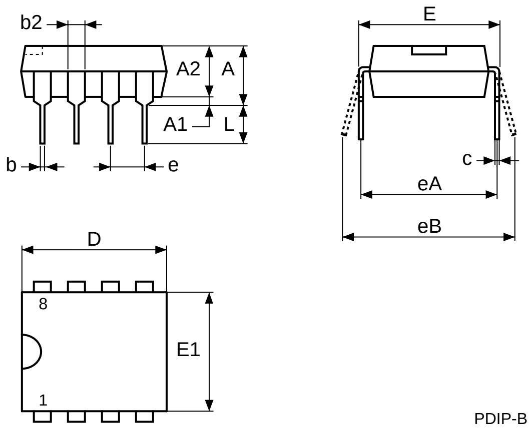


Figure 18. Output Timing



PACKAGE MECHANICAL

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline

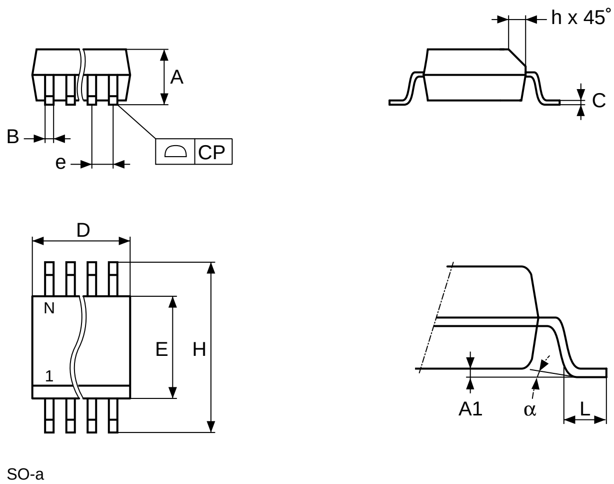


Notes: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline

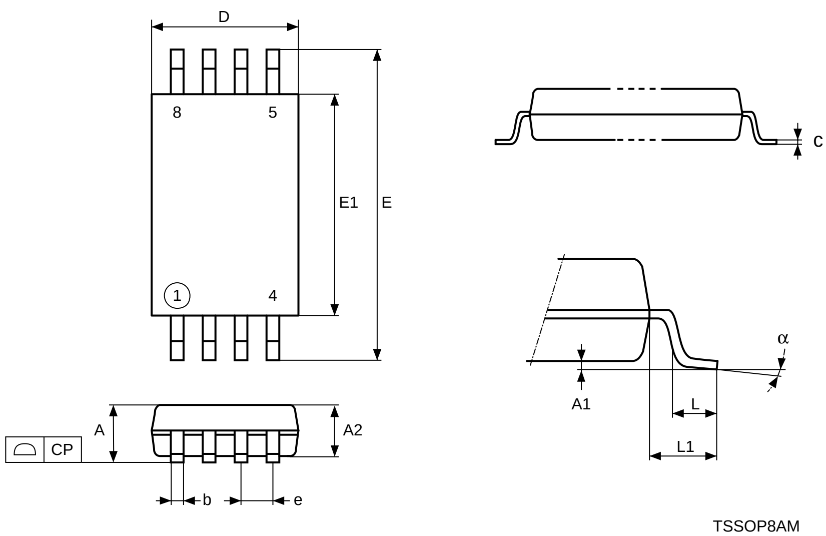


Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline



Notes: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

PART NUMBERING

Table 21. Ordering Information Scheme

Example: M95040 – W MN 6 TR

Device Type

M95 = SPI serial access EEPROM

Device Function[3]

040 = 4 Kbit (512 x 8)

020 = 2 Kbit (256 x 8)

010 = 1 Kbit (128 x 8)

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V

W = V_{CC} = 2.5 to 5.5V

S[2] = V_{CC} = 1.8 to 3.6V

Package

BN = PDIP8

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

Temperature Range

6 = –40 to 85 °C

3[1] = –40 to 125 °C

5 = –20 to 85 °C

Option

TR = Tape & Reel Packing

Note: 1. Temperature range available only on request.
2. The -S version (V_{CC} range 1.8 V to 3.6 V) only available in temperature range 5.
3. All devices use a positive clock strobe: Serial Data In (D) is strobed on the rising edge of Serial Clock (C) and Serial Data Out (Q) is synchronized from the falling edge of Serial Clock (C).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 22. Document Revision History

Date	Rev.	Description of Revision
10-May-2000	2.2	s/issuing three bytes/issuing two bytes/ in the 2nd sentence of the Byte Write Operation
16-Mar-2001	2.3	Human Body Model meets JEDEC std (Table 2). Minor adjustments to Figs 7,9,10,11 & Tab 9. Wording changes, according to the standard glossary Illustrations and Package Mechanical data updated
19-Jul-2001	2.4	Temperature range ‘3’ added to the -W supply voltage range in DC and AC characteristics
11-Oct-2001	3.0	Document reformatted using the new template
26-Feb-2002	3.1	Description of chip deselect after 8th clock pulse made more explicit
27-Sep-2002	3.2	Position of A8 in Read Instruction Sequence Figure corrected. Load Capacitance C_L changed
24-Oct-2002	3.3	Minimum values for tCHHL and tCHHH changed.
24-Feb-2003	3.4	Description of Read from Memory Array (READ) instruction corrected, and clarified